REMARKS

Applicants respectfully request reconsideration of the application in view of the following remarks.

EXAMINER INTERVIEW

An interview was held between the Examiner and the Applicants' undersigned attorney on May 18, 2006. Applicants' undersigned attorney would like to thank the Examiner for this interview.

INFORMATION DISCLOSURE STATEMENT

The Examiner indicated that the Information Disclosure Statement (IDS) submitted on February 27, 2006, fails to comply with 37 C.F.R. § 1.98(b)(5), as the reference "NPL, 'A New Type of Curvature-Compensated CMOS Bandgap Voltage Reference,' by Shu Yuan Chien et al." did not list the page numbers. **Applicants would like to point out that this reference did not include page numbers and, therefore, page numbers were not listed on the IDS (although the total number of pages was indicated on the IDS).** Accordingly, Applicants respectfully request that the Examiner consider this reference and return an initialed copy of the IDS indicating such consideration.

OBVIOUSNESS REJECTION UNDER 35 U.S.C. § 103 BASED ON US PATENT 6,172,611 TO HUSSAIN ET AL. IN VIEW OF US PATENT 5,675,297 TO GOSE ET AL.

Claims 37, 44, 45, 52, 53, and 60 were rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent 6,172,611 to Hussain et al. (hereinafter "Hussain") in view of United States Patent 5,675,297 to Gose et al. (hereinafter "Gose"). Applicants respectfully traverse this rejection as set forth below.

To reject a claim or claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. M.P.E.P. § 2142. When establishing a prima facie case of obviousness, the Examiner must set forth evidence showing that the following three criteria are satisfied:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references (or references when combined) must teach or suggest all the claim limitations.
> M.P.E.P. § 2143.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on the applicant's disclosure. M.P.E.P. § 2142 (citing *In re Vaeck*, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991)). Also, the evidentiary showing of a motivation or suggestion to combine prior art references "must be clear and particular." *In re Dembiczak*, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999).

A prima facie case of obviousness has not been set forth with respect to any of the claims for at least the following reasons: (1) Hussain and Gose, either individually or in combination, fail to disclose all of the claim limitations; and (2) there is no motivation to modify the teachings of Hussain and/or Gose to arrive at the claimed embodiments. Each of these issues is discussed in turn below.

Hussain and/or Gose Fail to Disclose All Claim Limitations

Hussain discloses a system level solution for monitoring the thermal state of a computer system. Column 2, Lines 60-67; Column 3, Lines 50-53. With reference to FIG. 1 of Hussain, a system 100 includes an embedded controller 110, a CPU chipset 120, a CPU 130 having a temperature sensor 132, a thermal management IC 140, a DC fan 160 and fan controller 150, and a power supply 170. Column 4, Lines 1-17. The temperature sensor 132 on CPU 130 is coupled with the thermal management IC 140, which includes its own on-board temperature sensor 146 for sensing a local temperature. Column 4, Lines 18-37. The embedded controller 110, which is controlled by the operating system of system 100, controls a CPU thermal management software module, with the assistance of chipset 120 and thermal management IC 140. Column 6, Lines 12-19.

The thermal management IC 140 includes a number of temperature setpoints, both software and hardware. Column 4, Lines 38-52. When a signal received from the CPU temperature sensor 132 (or from the on-board temperature sensor 146) indicates that a software temperature setpoint has been exceeded, the thermal management IC 140 issues an "ALERT#" signal to the embedded controller 110, and it is the embedded controller 110 that initiates any counter measures. Column 4, Lines 56-65; Column 7, Lines 21-66; FIG. 3. For example, the embedded controller 110 may direct the fan controller 150 to power up the fan 160, or the embedded controller 110 may direct the chipset 120 to throttle down the speed of a system clock signal 122 provided by the chipset to the CPU 130. Column 4, Line 65 through Column 5, Line 5; Column 5, Line 29 through Column 6, Line 8. When a signal received from the CPU temperature sensor 132 (or from the on-board temperature sensor 146) indicates that a hardware temperature setpoint has been exceeded, the thermal management IC 140 provides a shutdown signal to the power supply 170, and the power supply 170 then performs any necessary countermeasures (e.g., powering down the CPU 130). Column 5, Lines 13-22; Column 7, Lines 21-66; FIG. 3.

In sum, the CPU 130 includes a temperature sensor 132, but does not include any other elements of a thermal management system. Further, although the thermal management IC's on-board temperature sensor 146 may trigger countermeasures (see FIG. 3 of Hussain and accompanying text), those countermeasures are directed at the CPU 130. Thus, Hussain does not teach a thermal management system for an integrated circuit die, wherein the elements of the thermal management system are placed directly on the die itself. Rather, Hussain teaches a system level thermal management solution that is dispersed across multiple components of a computer system (e.g., the embedded controller 110, the chipset 120, the CPU 130, and the thermal management IC 140).

Gose is directed to a power output device having thermal shutdown protection. Column 2, Lines 41-47. More specifically, Gose discloses a conditional protection circuit 10 having a pulse-width modulation (PWM) circuit 12 and a thermal shutdown circuit 20. Column 3, Lines 14-24; FIG. 1. The thermal shutdown circuit 20 includes circuitry for detecting a die temperature and producing a fault signal when the temperature exceeds a predetermined limit. Column 3, Lines 24-27.

In contrast to the cited art, independent claim 37 of the present application recites:

> 37. A thermal management system for an integrated circuit die comprising:
>
> a temperature sensor **formed directly on the die**, the temperature sensor having an output;
>
> a power modulation element **formed directly on the die**, the power modulation element to reduce power consumption of the die in response to the output of the temperature sensor;
>
> a control element **formed directly on the die**, the control element including at least one register to provide an enable/disable bit for the thermal management system; and
>
> a visibility element **formed directly on the die**, the visibility element to indicate a status of the output of the temperature sensor.

Each of independent claims 45 and 53 recite some limitations similar to those recited in claim 37.

Thus, the claimed embodiments are directed to a die-level thermal management system for an integrated circuit die, wherein a temperature sensor, a power modulation element, a control element, and a visibility element of the thermal management system are all disposed directly on the die whose thermal characteristics are being monitored. These features of the claimed embodiments are not disclosed by Hussain and Gose, either individually or in combination. Rather, the cited art discloses a system-level thermal management system that is distributed across multiple, discrete components of a computer system (e.g., the embedded controller 110, the chipset 120, the CPU 130, and the thermal management IC 140).

It is further noted that the claimed die-level thermal management systems do not include many of the separate components disclosed in the cited art (e.g., the thermal management IC 140), and "**the omission of an element and retention of its function is an indicia of unobviousness**." M.P.E.P. § 2144.04(II)(B) (citing *In re Edge*, 149 U.S.P.Q. 556 (CCPA 1966)) (emphasis added).

No Motivation Exists to Modify the Cited References to Arrive at the Claimed Embodiments

The motivation to modify the teachings of a reference (or references) to arrive at the Applicants' claimed embodiments can come from two sources: (a) either the references themselves, or (b) the knowledge generally available to one of ordinary skill in the art. Further, the evidentiary standard for setting forth a motivation to modify references to arrive at the claimed embodiments it that evidence of such a motivation to modify (or combine) references "**must be clear and particular.**" *In re Dembiczak*, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999) (emphasis added). As the Court of Appeals for the Federal Circuit has warned:

> Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is **rigorous application** of the requirement for a showing of the teaching or motivation to combine [or modify] prior art references.
>
> ****
>
> Combining [or modifying] prior art references without evidence of such a suggestion, teaching, or motivation **simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability** – the essence of hindsight. *In re Dembiczak*, 50 U.S.P.Q.2d at 1617 (emphasis added).

Motivation to Modify References Not Found in References Themselves

Any assertion that Hussain and Gose contain a motivation to modify their respective teachings to arrive at the claimed embodiments is inconsistent with these disclosures.

In regards to Hussain, as specifically stated in the SUMMARY section of this reference:

> It has been discovered that a thermal management technique using a software and hardware programmable integrated circuit configured to receive a **remote temperature sensing** signal provides **the advantages of remote temperature sensing**, the flexibility of software programmability, and the reliability of hardware programmability. Column 2, Lines 41-46.

Clearly, as indicated in the passage above, Hussain is directed at and discloses only a temperature detection scheme wherein the temperature is sensed by a temperature sensor located remote from other components of the thermal management system. More specifically, other than a temperature sensing diode (item 132 in FIG. 1) located on the CPU, all other components of the thermal management approach disclosed in Hussain are located remote from the CPU.

Another passage from Hussain sheds additional light on the scope of this reference's disclosure:

> One exemplary thermal management IC 140 is shown in FIG. 4. The TC1066 is available from [the assignee of the Hussain patent]. The TC1066 is a serially programmable, monolithic temperature sensor optimized **for monitoring modern high performance CPUs** with on-board integrated thermal diodes. Column 8, Lines 25-30.

This passage clearly indicates that the thermal management IC 140 is one of many components of a thermal management system for monitoring the thermal characteristics of a separate integrated circuit device – i.e., a "modern high performance CPU". It is also noteworthy that the aforementioned product (i.e., the "TC1066" thermal management IC) is a product available from the assignee of the Hussain patent. The inventors and assignee of Hussain would certainly not intend, or suggest in their patent, that the disclosed thermal monitoring system be integrated onto the CPU itself, thereby eliminating the need for their own product.

Regarding Gose, as noted above, this disclosure is directed to a power device. There is no suggestion in this reference that any additional features are needed to satisfy the needs of such a device. Rather, all that appears necessary is the disabling of device 32 from conducting current. Column 4, Lines 9-12.

In sum, neither Hussain or Gose, either individually or in combination, contain any motivation to modify their respective teachings to arrive at the claimed embodiments. It is emphasized again that evidence of such a motivation must be "clear and particular."

Motivation to Modify References Not Found in the Knowledge Generally Available to One of Ordinary Skill in the Art

One must go back in time 5-plus years to the filing date of Applicants' disclosure to assess the knowledge generally available to one of ordinary skill in the art. Assuming Hussain (which discloses a thermal management scheme distributed across multiple components) and Gose (which is directed to a power delivery device) represent the state of the art, it would be a substantial leap to modify Hussain and/or Gose to arrive at the claimed embodiments. Applicants assert that one of ordinary skill in the art would not have been motivated – prior to the filing date of Applicants' disclosure – to make such a substantial leap. Once again, the requisite evidentiary showing of such a motivation must be "clear and particular."

Summary

For at least the reasons set forth above, Applicants assert that the Examiner has failed to set forth a prima facie case of obviousness with respect to independent claims 37, 45, and 53 based upon Hussain and Gose, either individually or in combination. Also, if an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 38-44, 46-52, and 54-60 are allowable as depending from nonobvious independent claims 37, 45, and 53, respectively.

CONCLUSION

Applicants submit that claims 37-60 are in condition for allowance and respectfully request allowance of such claims.

Please charge any shortages and credit any overages to our Deposit Account No. 02-2666.

Respectfully submitted,

Date: May 19, 2006

/Kerry D. Tweet/
Kerry D. Tweet, Reg. No. 45,959

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025
(503) 684-6200

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail on the below date with sufficient postage in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

Signature: Theresa Belland 5/19/06
Theresa Belland Date